11/06/2002 09/992,387

11jun02 14:18:25 User267149 Session D134.1

File 342:Derwent Patents Citation Indx 1978-01/200210
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*File 342: Price changes as of 1/1/02. Please see HELP RATES 342.

? S PN=US 5928458
? MAP PN/CT=
? MAP PN/CG=

CITATION SEARCH

? EXS SD065
? EXS SD066
? S S2:S3
? MAP PN

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

Set	Items	Description
S1	8	PN=DE 19905807 + PN=DE 3829538 + PN=DE 68911495 + PN=DE 69-009088 + PN=DE 69022087 + PN=DE 69102919 + PN=DE 69222905 + P-N=DE 69316159 + PN=EP 372880 + PN=EP 387066 + PN=EP 388011 + -PN=EP 449496 + PN=EP 528171 + PN=EP 596393
S2	21	PN=EP 880170 + PN=EP 930645 + PN=JP 11040609 + PN=JP 20001-14310 + PN=JP 2112250 + PN=JP 2523250 + PN=JP 2586154 + PN=JP 3016147 + PN=JP 3029207 + PN=JP 3051617 + PN=JP 3108734 + PN=-JP 3290936 + PN=JP 5239180 + PN=JP 6224258
S3	9	PN=KR 129500 + PN=KR 9302935 + PN=KR 9310722 + PN=KR 94105-37 + PN=US 4749120 + PN=US 5001542 + PN=US 5027995 + PN=US 50-71787 + PN=US 5120665 + PN=US 5296063 + PN=US 5471096 + PN=US 5739053 + PN=US 5843251 + PN=US 6096575
S4	3	PN=US 6113728 + PN=WO 200048242
S5	23	S1:S4
S6	0	S5 AND ((BALL()GRID OR LAND()GRID OR PAD()GRID OR PIN()GRI-D)(3N)ARRAY? ?)
S7	0	S5 AND ((BALL()GRID OR LAND()GRID OR PAD()GRID OR PIN()GRI-D))
S8	0	S5 AND (100(W)(MU OR MICRON? ?))
S9	0	S5 AND (INTEGRAT??????(2N)(CIRCUIT??? OR IC))
S10	18	S5 AND (((THIN()FILM???) OR LAYER??? OR COAT??? OR SUBSTRA-T????? OR MATERIAL? ? OR SUBSTANCE? ? OR (UNDERL????(2N)LAYER-???) OR BASE? ?))
S11	4	S10 AND (INSULAT????? OR MC=U11-C08A6)
S12	0	S10 AND INTERPOSER? ?
S13	2	S10 AND ((POLYIMIDE? ? OR (SYNTHETIC? ?(3N)RASIN) OR (POLY-MERIC(3N)RASIN? ?) OR (HEAT??? OR WEAR OR CORROSION???)(4N)RE-SIST???????) OR MC=VO4-RO7C)
S14	2	S13 NOT S11
S15	2	S5 AND ((SOLDER??? OR FUSIBLE(2N)ALLOY? ? OR BOND???? OR J-OIN?????? OR CEMENT????)(2N)(BALL? ? OR BUMP? ?))
S16	1	S15 NOT S11,S13
S17	3	S5 AND (GOLD OR AU)(2N)BUMP? ?
S18	1	S17 NOT S11,S13,S16
S19	1	S5 AND (((COPPER OR CU)(2N)(BALL? ? OR BUMP? ?)) OR ((NICK-EL OR NI)(2N)(BALL? ? OR BUMP? ?)) OR ((PALLADIUM OR PD)(2N)(-BALL? ? OR BUMP? ?)))
S20	1	S19 NOT S18

11/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008390078
WPI Acc No: 1990-277079/**199037**
Related WPI Acc No: 1990-180640
XRAM Acc No: C90-119700
XRPX Acc No: N90-214119

Connecting semiconductor chip to PCB - using **insulating**, heat and pressure curable adhesive film contg. liq. polyepoxy resin, solid resin and microcapsule type curing agent

Patent Assignee: HITACHI CHEM CO LTD (HITB)
Inventor: GOTO Y; NAKAJIMA A; TSUKAGOSHI I; YAMAGUCHI Y
Number of Countries: 007 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5843251	A	19981201	US 90490915	A	19900309	199904
			US 92853868	A	19920320	
US 6113728	A	20000905	US 90490915	A	19900309	200044
			US 92853868	A	19920320	
			US 95464118	A	19950605	

Priority Applications (No Type Date): EP 90302493 A 19900308; JP 8956771 A 19890309
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5843251	A			B32B-031/00	Cont of application US 90490915
US 6113728	A			B32B-031/00	Cont of application US 90490915 Div ex application US 92853868 Div ex patent US 5843251

Abstract (Basic): EP 387066 A

Electrically connecting circuits in which at least one circuit is provided on an **insulating layer** and has projecting electrodes which are deformable under pressure in the circuit connecting operation involves the interposition between the circuits of an **insulating** heat and pressure curable adhesive film with less than 0.5 wt% volatile content, of less than 50 microns in thickness, and comprising (i) a liq. epoxy resin, (ii) a solid resin having at least one functional gp., and (iii) a microcapsule type curing agent.

ADVANTAGE - Application of heat and pressure to a sandwich consisting of a semiconductor chip, the adhesive film and a circuit on a **substrate** results in simultaneous electrical connection and bonding, with excess adhesive forming a protective bead round the chip. The characteristics of the adhesive permit live testing of the circuit while the adhesive is in a half-cured state (claimed). (14pp Dwg.No.1a/8)

Abstract (Equivalent): EP 387066 B

A process for electrically connecting circuits wherein at least one circuit is provided on an **insulating layer** and has a plurality of projecting electrodes which are deformable under pressure

in the circuit connecting operation, wherein an **insulating** adhesive having a volatile content of 0.5% or less by weight and comprising (i) a liquid epoxy resin, (ii) a solid resin having one or more functional groups for improving adhesiveness and compatibility with epoxy resin and (iii) a microcapsule curing agent comprising encapsulated particles with a curing agent core, said **insulating** adhesive in the form of a film having a thickness of 50 microns or less is interposed between the circuits and is substantially cured after the projecting electrodes have been contacted with the opposing circuits by applying heat and pressure at the time of connection.

11/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04552358

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 06-224258 [**JP 6224258** A]
PUBLISHED: August 12, 1994 (19940812)
INVENTOR(s): KAWAKITA TETSUO
HATADA KENZO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-264517 [JP 93264517]
FILED: October 22, 1993 (19931022)
JOURNAL: Section: E, Section No. 1628, Vol. 18, No. 590, Pg. 78, November 10, 1994 (19941110)

ABSTRACT

PURPOSE: To provide a connection system which has high reliability of connection when a transfer system for forming a metal protrusion on the electrode of a semiconductor element easily and at a low cost.

CONSTITUTION: A metal protrusion 22 formed on a **substrate** used for a metal protrusion and the Al electrode 24 of a semiconductor element 23 are pressed and heated in contact with each other so as to be interconnected with the alloying of the metal protrusion 22 and the Al electrode 24, and then the metal protrusion 22 is transferred to the Al electrode 24. After that, the metal protrusion 22 and a wiring electrode 27 are alloyed again by pressing and heating with higher pressure and higher temperature being applied thereto for longer time than those in the previous process. After that, the metal protrusion 22 and the wiring electrode 27 are interconnected by solidifying a photo-curing **insulating** resin 29. Thereby, the metal protrusion 22 before connected to the wiring electrode 27 is prevented from being greatly deformed and at the same time the strength of connection between the Al electrode and the metal protrusion is increased.

11/3,AB/3 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03445834
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 03-108734 [**JP 3108734** A]
PUBLISHED: May 08, 1991 (19910508)
INVENTOR(s): SAITO MASAYUKI
MORI MIKI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-163196 [JP 89163196]
FILED: June 26, 1989 (19890626)
JOURNAL: Section: E, Section No. 1096, Vol. 15, No. 304, Pg. 51, August 05, 1991 (19910805)

ABSTRACT

PURPOSE: To mount a semiconductor element on an **insulating substrate** in a face down state, to improve the reliability of a connecting part and to facilitate the replacement of the semiconductor element by bonding a gold bump which is provided on the electrode of the semiconductor element to a wiring pattern of the **substrate** through a metal which contains indium.

CONSTITUTION: A semiconductor element 11 is mounted on a **substrate** 21 on which a wiring pattern 22 is formed in a face down state. In this device, a gold bump 12 is provided on the electrode of the semiconductor element 11. The gold bump 12 and the wiring pattern 22 are bonded througb a metal 13 containing indium. For example, the gold bump 12 is formed on the electrode of the semiconductor element 11. The semiconductor element on the side of the gold bump 12 is immersed into fused liquid of metal containing indium. Thereafter, the semiconductor element 11 is separated from the fused element 11, and the metal 13 having the spherical surface shape containing indium is formed on the gold bump 12. Then, the metal 13 having the spherical surface shape and the wiring pattern 22 of the **substrate** 21 are brought into contact. They are heated, compressed and bonded. Thereafter, a resin 14 is impregnated in the gap between the element 11 and the **substrate** 21 and hardened

11/3,AB/4 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03353247

CONNECTION OF CIRCUITS AND ADHESIVE FILM USED THEREFOR

PUB. NO.: 03-016147 [**JP 3016147** A]
PUBLISHED: January 24, 1991 (19910124)
INVENTOR(s): TSUKAGOSHI ISAO
YAMAGUCHI YUTAKA
NAKAJIMA ATSUO
GOTO YASUSHI
APPLICANT(s): HITACHI CHEM CO LTD [000445] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-050168 [JP 9050168]
FILED: March 01, 1990 (19900301)
JOURNAL: Section: E, Section No. 1052, Vol. 15, No. 135, Pg. 23, April 04, 1991 (19910404)

ABSTRACT

PURPOSE: To realize a connection whose reliability is excellent by a method wherein a bump is provided with a deformable property and a specific adhesive film is used.

CONSTITUTION: An adhesive 7 is formed between electrodes 2 protruding from a main face 6 of an electronic component 1 such as a semiconductor chip or the like and circuits 4 formed on an **insulating substrate** 3; connection points of the bumps 2 and the circuits 4 are aligned; the bumps 2 and the circuits 4 are brought into contact by a heating and pressurization operation when they are connected; the adhesive 5 whose viscosity has been lowered is excluded to the outside of contact parts; an irregularity in a height is flattened by pressurizing and deforming the bumps 2. The adhesive 5 used at this time is an adhesive whose thickness is 50.mu.m or lower, whose volatile matter is 0.5wt.% or lower and which is a film shape at room temperature. Thereby, it is possible to realize an electrical connection whose reliability is high by a simple and easy method of the heating and pressurization operation by using the **insulating** adhesive 5.

14/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013184093
WPI Acc No: 2000-355966/**200031**
XRPX Acc No: N00-267070
Flip-chip bonding optimization condition detection method for use in thermocompression bonding test device, involves maintaining contact **resistance** and **heating** temperature of chip at fixed values for preset time
Patent Assignee: NIPPON MOTOROLA KK (MOTI); MOTOROLA INC (MOTI)
Inventor: KATAHIRA T; OKADA Y
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000114310	A	20000421	JP 98276943	A	19980930	200031	B
US 6096575	A	20000801	US 99384934	A	19990826	200039	

Priority Applications (No Type Date): JP 98276943 A 19980930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000114310	A		7	H01L-021/60	
US 6096575	A			H01L-021/44	

Abstract (Basic): **JP 2000114310** A
Abstract (Basic):

NOVELTY - The semiconductor chip (12) is pressed at preset velocity to contact a **substrate** (11) via a bonding **material** till the contact resistance reaches a preset value. The temperature of the **substrate** is increased till the temperature of semiconductor reaches above a fixed temperature. After maintaining the contact resistance and temperature at above fixed values for certain time, they are reduced.

USE - For detecting the optimum pressure and optimum temperature in flip-chip bonding of thermocompression bonding test device.

ADVANTAGE - Pressure and heating temperature which makes the contact resistance small in case flip-chip bonding using a bonding **material**, is easily detected by rising the contact resistance to a set value and rising the temperature of semiconductor chip above a fixed temperature.

DESCRIPTION OF DRAWING(S) - The figure shows the thermocompression bonding device.

Substrate (11)
Semiconductor chip (12)

14/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008293639
WPI Acc No: 1990-180640/**199024**
Related WPI Acc No: 1990-277079
XRAM Acc No: C90-078385
XRPX Acc No: N90-140382
Circuit connection adhesive for semiconductor chips - comprising polyepoxy resin adhesive, **coated** curing agent particles and pressure-deformable electroconductive particles
Patent Assignee: HITACHI CHEM CO LTD (HITB)
Inventor: GOTO Y; NAKAJIMA A; TSUKAGOSHI I; YAMAGUCHI Y; NAKAJIMAK A
Number of Countries: 007 Number of Patents: 011
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5001542	A	19910319	US 89443169	A	19891130	199114
US 5120665	A	19920609	US 89443169	A	19891130	199226
			US 91671472	A	19910319	
US 5843251	A	19981201	US 90490915	A	19900309	199904
			US 92853868	A	19920320	
US 6113728	A	20000905	US 90490915	A	19900309	200044
			US 92853868	A	19920320	
			US 95464118	A	19950605	

Priority Applications (No Type Date): JP 8969973 A 19890322; JP 88307618 A 19881205; JP 895540 A 19890112; JP 895541 A 19890112; JP 89314647 A 19891204; JP 8956771 A 19890309
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5120665	A		16	H01L-021/326	Div ex application US 89443169
					Div ex patent US 5001542
US 5843251	A			B32B-031/00	Cont of application US 90490915
US 6113728	A			B32B-031/00	Cont of application US 90490915
					Div ex application US 92853868
					Div ex patent US 5843251

Abstract (Basic): EP 372880 A

Compsn. for use in circuit connection comprises (A) an epoxy resin-contg. reactive adhesive; (B) **coated** particles with a nucleus of curing agent; (C) 0.1-15 vol. % (**based** on vol. of (A)+(B) of pressure deformable electroconductive particles of ave. particle size larger than that of particles (B), and opt. (D) rigid particles of ave. particle size smaller than that of particles (B).

Pref. the compsn. has Cl ion concn. in extracted water 15ppm or less and an activation temp. of 70-200 deg.C.

USE/ADVANTAGE - Compsn. is used, for electrically connecting electrodes of a semiconductor chip to circuits of a **substrate** and fixing the chip to the **substrate** (e.g. a flexible circuit board). Bumpless connections can be made and reliable **heat resistant** connections are obtd. with the electroconductive particles packed at higher density than in prior techniques. (24pp

16/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008397222
WPI Acc No: 1990-284223/**199038**
XRPX Acc No: N90-219161
Semiconductor device using face-down bonding in mfr. - forms **bond** between gold **bumps** coated with indium tin bumps and wiring layer
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: MORI M; SAITO M
Number of Countries: 005 Number of Patents: 005

US 5071787	A	19911210	US 90477504	A	19900209	199201
			EP 90301542	A	19900214	

Priority Applications (No Type Date): JP 89163196 A 19890626; JP 8961634 A 19890314
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 388011	A				
Designated States (Regional): DE FR GB					
EP 388011	B1	E	14	H01L-021/60	
Designated States (Regional): DE FR GB					
DE 69022087	E			H01L-021/60	Based on patent EP 388011

Abstract (Basic): EP 388011 A

The semiconductor device includes a substrate (21) having a wiring layer (22) formed on its major surface, and a semiconductor element (11) having an electrode (12) formed on its major surface. The semiconductor element is mounted with its major surface facing the major surface of the substrate so that the wiring layer is bonded to the electrode. First bumps (13) of Au are formed on the electrode and second bumps (14), made of a metal contg. In are located between the first bump and the wiring layer to form an electrical and mechanical bond therebetween.

The substrate (21) may be a liquid crystal panel. In this case the second bumps are formed of In/Sn alloy. This alloy is deposited around a side wall of the first **bumps**. The **bonding** process is effected by pressing the second bumps into contact with the wiring layer whilst heating the second bumps to a temp. not exceeding their m.pt. Subsequent to electrical testing, the bonded region is impregnated with resin (15).

ADVANTAGE - Allows formation of good reliable bond prior to resin cure step. Thus it is not necessary to maintain pressure on aligned bonds during lengthy curing process and so productivity is improved. Semiconductor element is more easily removed. (13pp Dwg.No.1c/7

18/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009872901
WPI Acc No: 1994-152814/**199419**
XRPX Acc No: N94-120033
Mounting semiconductor chips during mfr using bumps, e.g.memory card, LCD or EL display contg LSI chips on PCB - transferring bumps from substrate using low temp. and pressure and welding chip to board using higher temp. and pressure.
Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA ELEC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU)
Inventor: HATADA K; KAWAKITA T
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5739053	A	19980414	US 93140473	A	19931025	199822
			US 95440991	A	19950515	

Priority Applications (No Type Date): JP 92288533 A 19921027
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5739053	A		17	H01L-021/283	CIP of application US 93140473

Abstract (Basic): EP 596393 A
The substrate is prepared with **gold bumps** formed by electrolytic plating etc. Semiconductor device (23) is aligned with the bumps (22). The electrodes and bumps are brought into contact and bonded together. Subsequently the bumps (22) are peeled off from the substrate and remain bonded to the respective aluminium electrodes (24).
The semiconductor device (23) is subsequently placed on a circuit board (28) with the bumps (22) aligned with wiring electrodes (27). Then, the bumps (22) and the wiring electrodes (27) are bonded together more securely by the application of a larger pressure at a higher temperature than in the preceding process, allowing re-alloying.
ADVANTAGE - Forms bonds which are stronger and more reliable at high temp.
Dwg.1g/6
Abstract (Equivalent): EP 596393 B
The substrate is prepared with **gold bumps** formed by electrolytic plating etc. Semiconductor device (23) is aligned with the bumps (22). The electrodes and bumps are brought into contact and bonded together. Subsequently the bumps (22) are peeled off from the substrate and remain bonded to the respective aluminium electrodes (24).
The semiconductor device (23) is subsequently placed on a circuit board (28) with the bumps (22) aligned with wiring electrodes (27). Then, the bumps (22) and the wiring electrodes (27) are bonded together more securely by the application of a larger pressure at a higher temperature than in the preceding process, allowing re-alloying.
ADVANTAGE - Forms bonds which are stronger and more reliable at

20/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013415087
WPI Acc No: 2000-587025/**200055**
XRAM Acc No: C00-174909
XRPX Acc No: N00-434482
Production of electrical conducting connections comprises forming **palladium** connection **bumps** on contacts, pressing bumps onto conducting path structure, and joining the electronic components to the substrate
Patent Assignee: KSW MICROTEC GES ANGEWANDTE MIKROTECHNIK (KSWM-N)
Inventor: KRIEBEL F; SEIDOWSKI T; SADOWSKI G
Number of Countries: 024 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200048242	A1	20000817	WO 2000DE417	A	20000211	200055	B
DE 19905807	A1	20000831	DE 1005807	A	19990211	200055	
EP 1155445	A1	20011121	EP 2000914028	A	20000211	200176	
			WO 2000DE417	A	20000211		

Priority Applications (No Type Date): DE 1005807 A 19990211
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200048242	A1	G	31	H01L-021/60	
	Designated States (National): IL JP US ZA				
	Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GR IE IT LU MC NL PT SE				
DE 19905807	A1			H01L-021/60	
EP 1155445	A1	G		H01L-021/60	Based on patent WO 200048242
	Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE				

Abstract (Basic): **WO 200048242** A1
Abstract (Basic):
NOVELTY - Production of electrical conducting connections between individual contacts of electronic components (1) having a conducting path structure formed on the substrate (4) comprises forming connection bumps (2) made predominantly of palladium on the contacts by currentless deposition, pressing the bumps directly onto the conducting path structure, and permanently joining the electronic components to the substrate using a material (5) exerting a pressure or pulling force as a result of a reduction of volume or a polymer film.
USE - For contacting electronic components with printed circuit boards, chip cards or flexible support materials.
ADVANTAGE - The process is cost-effective and better transfer safety in an electrically conductive connection is achieved.
DESCRIPTION OF DRAWING(S) - The drawing shows a section through part of a chip card.
electronic component (1)
connection bumps (2)